Kontron User's Guide

DIMM-PC/386-I/IE

Document Revision 129

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1 User Information

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Asia	Europe	North/South America
Kontron Asia Inc.	Kontron Embedded Modules GmbH	Kontron America
4F, No.415, Ti-Ding Blvd., NeiHu District, Taipei 114, Taiwan	Brunnwiesenstr. 16 94469 Deggendorf – Germany	14118 Stowe Drive Poway, CA 92064-7147
Tel: +886 2 2799 2789	Tel: +49 (0) 991-37024-0	Tel: +1 (888) 294 4558
Fax: + 886 2 2799 7399	Fax: +49 (0) 991-37024-333	Fax: +1 (858) 677 0898
mailto:sales@kontron.com.tw	mailto:sales-kem@kontron.com	mailto:sales@us-kontron.com

2 Introduction

2.1 Important Information

This user guide provides information about the two different versions of the DIMM-PC/386. Below is a list of the corresponding article numbers for each version. Each version may be equipped with different options for onboard memory and onboard IDE compatible Flash hard disk.

- 08004-xxxx-xx-0 DIMM-PC/386-I (with IDE compatible flash)
- 08004-xxxx-xx-1 DIMM-PC/386-IE (with IDE compatible flash and Ethernet)

When reading this user guide the user must be aware of which version of the DIMM-PC/386 they have. The information within this user guide covers two versions of the DIMM-PC/386.When certain information, within this user guide, only applies to a particular version of DIMM-PC/386 then it will be stated.

For example: **Onboard 10BaseT Ethernet (DIMM-PC/386-IE only)**

2.2 DIMM-PC/386-I/IE

The DIMM-PC/386-I/IE integrates the complete functionality of an 80386 SX motherboard with a CPU, system BIOS, 2MB-8MB of DRAM, keyboard controller, and real-time clock. It also offers peripheral functions such as COM1, COM2, LPT1, floppy disk, and IDE hard-disk interfaces, which are available through the DIMM-PC bus connector that is integrated on the board. The system runs at CPU clock speeds of between 10MHz up to 40MHz and has a default speed of 33MHz. You can adjust the CPU clock speed by using the AMI BIOS setup.

The DIMM-PC/386-I/IE includes an onboard, 4MB, 8MB, or 16MB IDE-compatible Flash hard disk, which you can configure as the master IDE device. The DIMM-PC/386-IE includes an onboard 10BaseT Ethernet controller.

2.3 Bus Connector

The pinout of the DIMM-PC bus connector corresponds in large part to the pinout of a standard ISA bus. Only latchable address bus LA[17..23] and DMA signals 1,3,4, and 6 are not connected to the DIMM-PC bus. In addition, the DIMM-PC bus offers peripheral functions such as COM1, COM2, LPT1, floppy interface, and an IDE hard-disk interface.

2.4 DIMM-PC Architecture

The application-specific portion of a standard embedded application typically requires low pin count components such as relays, power supplies and A/D-converters. An embedded PC requires components of much higher pin-count and higher density circuit boards. The DIMM-PC concept separates the high-density circuit board of the embedded PC from the low density, often two-layer, application-specific baseboard.

To simplify the connection of the peripheral components, such as A/D converters, a programmable chip-select-signal has been defined on the DIMM-PC bus. This chip-select-signal can be adjusted in the BIOS setup of the PC for corresponding I/O addresses. With a single external TTL component, up to eight I/O components can be triggered. In the regular ISA bus, the user has to connect 20 pins to a GAL to select an external component. The programmable chip select decodes unnecessary ISA bus address signals. This makes triggering the external bus-buffer components possible.

To address the drawback of a higher price for a PC solution, the DIMM-PC performs without discrete peripheral connectors, significantly reducing the cost. In other PC solutions, such as PC/104, connectors and their assembly are a significant part of the manufacturing costs. In "low end" 386SX-solutions, these costs can be as much as 25%. Because the DIMM-PC performs without connectors, these costs are significantly decreased and the PC can be integrated on a smaller board surface. The reduction in the number of steps necessary in manufacturing and assembling the component group is another cost-decreasing factor.

The two-sided reflow process, as well as exclusion of the wave-solder process, serves to increase the yield in manufacturing and improve quality. The required SO-DIMM connector is a very inexpensive, standard component and is available from numerous manufacturers.

In designing the DIMM PC, special attention was directed toward its use in embedded applications. Moreover, its design was developed in co-operation with large-scale customers. Because most peripheral interfaces used in such applications are device-internal (in external interfaces, mainly special customized interfaces are used), the RS232 interface driver components have been excluded from the DIMM-PC, leading the interfaces as pure TTL signals to the outside. This further decreases additional costs, while enabling the user to have more flexibility when selecting the interface driver (RS485, RS422, RS232, TTY etc.) The power consumption of the PC architecture is reduced with highly integrated components. This also makes the system optimally adaptable with power-saving modes.

The PC in the DIMM-PC architecture also has minimized or eliminated some of the most critical disadvantages of the microcontroller:

- The DIMM-PC today needs less board surface than most micro-controller applications.
- The embedded PC cost has been drastically decreased by the DIMM-PC architecture.
- The DIMM-PC architecture has eliminated the complicated cabling of an embedded PC.

The user receives important advantages by using a DIMM-PC. Because of the 100% PC-compatibility, the user can begin the software development immediately on a standard PC. This is a factor that may influence the success of a product in today's market, where "time to market" is of high importance. As target hardware becomes available, it can be implemented with no obstacles to operation because it will be unnecessary to change the software. With the SO-DIMM-connector, an exchange for a more powerful type CPU is possible, increasing the scalability of the ultimate device. In the case of product information and new designs, the CPU may simply be superseded by a new DIMM-PC, saving redesign time. Through continuous development of the DIMM-PC modules, the cost for the life span of a product can be reduced, profiting users. The integrated IDE controller allows the user to work with normal PC tools with no need for hardware-specific drivers.

3 Specifications

3.1 Functional Specifications

Processor

- Intel 386SX processor – 10MHz - 40MHz (default speed runs at 33MHz). Single-chip implementation of Intel 386SX processor and ALi M1217B chipset.

Chipset

- Acer Labs, Inc. (ALi) - M6117C - single-chip implementation of Intel 386SX processor and ALi M1217B chipset.

Memory

- 2, 4, or 8MB DRAM

Onboard IDE compatible Flash hard disk with up to 16MB (always IDE master)

Two serial port interfaces: COM1 and COM2

- TTL signals, 16550 compatible

One parallel port interface (LPT1)

- EPP support
- Floppy interface

IDE hard-disk interface (external hard disk as slave)

Real-time clock

Keyboard controller

EEPROM for CMOS setup

I²C Bus (slave devices only)

5V only power supply

Watchdog timer

Onboard 10BaseT Ethernet (DIMM-PC/386-IE only)

3.2 Mechanical Specifications

The interconnection of a DIMM-PC board is achieved by plugging the board to the DIMM connector in a peripheral application. Following are the dimensions of the DIMM-PC board and a DIMM connector. Please refer to the Kontron DIMM-PC specification for additional information.

3.2.1 PCB Dimensions

➤ 67.6 mm x 40 mm (2.7" x 1.6")

3.2.2 Height

➤ 6 mm max

3.3 Electrical Specifications

3.3.1 Supply Voltage

➤ 5V DC +/- 5%

3.3.2 Supply Voltage Ripple

➤ 100 mV peak to peak 0 - 20 MHz

3.3.3 Suspend Supply Current (Typical)

➤ Suspend mode not supported

3.3.4 Supply Current (Typical)

➤ ≈300mA at 33MHz

3.3.5 Supply Current Battery (Maximum)

- < 5µA @ 3 V battery, 0.70°C with system power off
- < 2µA with system power on

3.4 Environmental Specifications

3.4.1 Temperature

- Operating: 0 to +65 C (*) (with appropriate airflow)
- Non-operating: -40 to +80 °C (non-condensing)

Note: *The maximum operating temperature is the maximum measurable temperature on any spot on the module's surface. You must maintain the temperature according to the above specification.*

3.4.2 Humidity

- Operating: 10% to 90% (non-condensing)
- Non-operating: 5% to 95% (non-condensing)

4 CPU, Chipset, and CPU

4.1 CPU

The DIMM-PC/386-I/IE contains an Acer Labs ALi - M6117C embedded controller. The M6117C is a highly integrated, low-voltage, single-chip implementation of an Intel 386SX Processor compatible microprocessor and an ALi M1217B chipset. The M6117C provides the Intel 386SX core and supports the EDO DRAM controller, including FP mode, coprocessor interface, ISA interface, and a peripheral interface.

The peripheral interface supports:

- Two cascaded 8237 Direct Memory Access (DMA) controllers
- 74612 memory mapper
- Two cascaded 8259 interrupt controllers
- 8254 programmer counter

The embedded microcontroller also includes:

- Built-in, real-time clock
- PS/2/AT keyboard controller
- Watchdog timer
- 16-bit GP I/O
- IDE hard-disk interface

4.2 Chipset

The ALi M1217B chipset is embedded in the ALI AM6117C microprocessor.

4.3 Super I/O

The DIMM-PC/386-I/IE contains the SMSC Super I/O (FDC37C669) Controller from Standard Microsystems Corp. The FDC37C669 includes:

- Two serial ports (COM3 and COM4)
- Two high-speed, NS16C550-compatible UARTs with send/receive, 16- byte FIFOs
- 230K and 460K baud support
- Programmable baud-rate generator
- 96 base I/O address and eight IRQ options

5 System Memory

The DIMM-PC/386-I/IE contains 2MB to 8MB of DRAM, which are integrated onboard.

6 ISA Bus

The DIMM-PC/386-I/IE supports the PC/104 16-bit ISA bus. The pinout of the DIMM-PC bus connector corresponds to the pinout of the ISA bus connector. The Latchable Address (LA) bus [17-23] and DMA signals 1, 3, 4, and 6 are not connected to the DIMM-PC bus.

6.1 Signals

6.1.1 SD<0:15>: System Data Bus

Bi-directional I/O pins.

This refers to signals that provide data bus bits 0 to 15 for peripheral devices. All 8-bit devices use SD<0:7> for data transfers. The 16-bit devices use SD<0:15>. To support 8-bit devices, the data on SD<8:15> will be gated to SD<0:7> during 8-bit transfers to these devices. The 16-bit CPU cycles will convert into two, 8-bit cycles for 8-bit peripherals.

6.1.2 SA<19:0>: System Address

Output from CPU modules and input to all other modules.

This refers to address bits 0:15 that address I/O devices. Address bits 0:19 address system memory. The 20 address lines, in addition to LA<17:23>, allow access of up to 16MB of memory. SA<0:19> are gated on the PC/104-bus when BALE is high and latched to the falling edge of BALE.

6.1.3 /SBHE: System Bus High Enable

This refers to output on CPU modules and input to other modules. The signal /SBHE indicates a transfer of data on the upper byte of the data bus (SD<8:15>). The 16-bit I/O devices use /SBHE to condition data bus buffers tied to SD<8:15>.

6.1.4 BALE: Bus Address Latch Enable

This refers to output from CPU modules and input on other modules. The signal BALE is an active high pulse, which generates at the beginning of a bus cycle that is initiated by a CPU module. It indicates when the SA<0:19>, LA<17:23>, AEN, and /SBHE signals are valid.

6.1.5 AEN: Address Enable

This refers to output from CPU modules and input to other modules. The signal AEN is an active high output that indicates a DMA transfer cycle. Only resources with an active /DACK signal should respond to the command lines when AEN is high.

6.2 Control Signal Group

6.2.1 /SMEMR System Memory Read

This refers to output from CPU modules and input to other modules. The signal /SMEMR instructs memory devices to drive data onto the data bus. The signal /SMEMR is active on memory-read cycles to addresses below 1MB.

6.2.2 /SMEMW: System Memory Write

This refers to output from CPU modules and input on other modules. The signal /SMEMW instructs memory devices to store the data present on the data bus. The signal /SMEMW is active on all memory-write cycles to addresses below 1MB.

6.2.3 /IOR: I/O Read

This refers to output from CPU modules and input on other modules. The signal /IOR instructs an I/O device to drive its data onto the data bus. The CPU or DMA controller may drive the data. /IOR is inactive (high) during refresh cycles.

6.2.4 /IOW: I/O Write

This refers to output from CPU modules and input on other modules. The signal /IOW instructs an I/O device to store present data on the data bus. The CPU or DMA controller may drive the data. The signal /IOW is inactive (high) during refresh cycles.

6.2.5 /IOCHCK: I/O Channel Check

This refers to output from CPU modules and input on other modules. The signal /IOCHCK is an active, low-input signal that indicates an error has taken place on the module bus. If /IOCHCK is enabled on the CPU module, an /IOCHCK assertion by a peripheral device generates a nonmaskable interrupt (NMI) to the processor.

6.2.6 IOCHRDY: I/O Channel Ready

This refers to output from CPU modules and input on other modules. The IOCHRDY is pulled low to extend the read or write cycles of any bus access when required. The CPU, DMA and refresh controllers can initiate the cycle. The default number of wait states for cycles initiated by the CPU is 4 for 8-bit peripherals and 1 wait state for 16-bit peripherals. One wait state is inserted as a default for all Direct Memory Access (DMA) cycles. Peripherals that cannot present read data or strobe in write data in this amount of time use IOCHRDY to extend the cycles.

This signal should not be held low for more than 2.5 us for normal operation. Any extension to more than 2.5 us does not guarantee proper DRAM memory contents because memory refresh is stopped while IOCHRDY is low.

6.2.7 /MEMCS16: 16 Bit Memory Chip Select

This refers to input to CPU modules and open collector output on other modules. The /MEMCS16 signal determines when a 16-bit to 8-bit conversion is needed for memory bus cycles. A conversion is done when the CPU module requests a 16-bit memory cycle and the /MEMCS16 line is high. If the /MEMCS16 line is high, 16-bit CPU cycles are automatically converted into two, 8-bit cycles on the bus. If /MEMCS16 is low, an access to peripherals is done via a 16-bit wide cycles.

6.2.8 /IOCS16: 16 Bit I/O Chip Select

This refers to input to CPU modules and open collector output to other modules. The /IOCS16 signal determines when a 16-bit to 8-bit conversion is needed for I/O-bus cycles. A conversion is done when the CPU module requests a 16-bit I/O cycle and the /IOCS16 line is high. If /I/OCS16 is high, 16-bit CPU cycles are converted into two, 8-bit cycles on the bus. If /I/OCS16 is low, access to peripherals is done via 16-bit wide cycles.

6.2.9 /REFRESH: Memory REFRESH

This refers to output to CPU modules and input to other modules. The signal /REFRESH pulls low whenever a refresh cycle initiates. A refresh cycle activates every 15.6 us to prevent loss of DRAM data.

6.2.10 /0WS: 0 Wait States

This refers to input to CPU modules and output to other modules. The 0 wait-state signal tells the CPU to complete the current bus cycle without inserting default wait states. By default, the CPU inserts four wait states for 8-bit transfers and one wait state for 16-bit transfers.

6.3 Special Function Signal Group

6.3.1 /MASTER

This signal is internally connected and is not to be used by external devices.

6.3.2 SYSCLK: System Clock

This refers to output from a CPU module and input to other modules. The signal SYSCLK is supplied by the CPU module and has a nominal frequency of about 8 MHz with 40-60 percent duty cycle. Different CPU modules can supply slower and higher frequencies. This signal is supplied at all times except when the CPU module is in sleep mode.

6.3.3 OSC: Oscillator Frequency

This refers to output from CPU modules and input to other modules. CPU modules supply OSC. They have a nominal frequency of 14.3 MHz and a duty cycle of 40-60 percent. This signal is supplied at all times except when the CPU module is in sleep mode.

6.3.4 RESETDRV: Bus RESET

This refers to output from CPU modules and input to other modules. This active high output is system-reset generated from CPU modules to reset external devices.

6.3.5 DRQ: DMA Request

This refers to CPU modules and outputs from other modules. External devices use the asynchronous DMA request inputs to indicate when they need service from the CPU modules' DAM controllers. DRQ<0:3> are used for transfers between 8-bit, I/O adapters and system memory. DRQ<5:7> are used for transfers between 16-bit, I/O adapters and system memory. DRQ4 is not available externally. All DRQ pins have pull-up resistors on CPU modules.

6.3.6 /DACK: DMA Acknowledge

This refers to outputs from CPU modules and inputs to other modules. DMA acknowledges 0-3 and 5-7 acknowledges DMA requests. They are low active.

6.3.7 T/C: Terminal Count

This refers to output from CPU modules and input to other modules. The active high output TC indicates that one of the DMA channels has transferred all data.

6.3.8 IRQ: Interrupt Requests

This refers to input to CPU modules and output to other modules. These are asynchronous interrupt request lines. IRQ0, 1, 2, 8 and 13 are not available as external interrupts because they are used internally on CPU modules. All IRQ signals are inactive high. The interrupt requests are prioritized. IRQ9 through IRQ12 and IRQ14 through IRQ15 have the highest priority (IRQ9 is the highest). IRQ3 through IRQ7 have the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the CPU acknowledges the interrupt request (interrupt-service routine).

7 Serial Communication Interface

The DIMM-PC/386-I/IE has two 16550 compatible serial ports, with TTL-level signals. You can configure the ports as COM1 and COM2.

7.1 Configuration

You can set the COM1 and COM2 serial ports to the base I/O-address 3F8h, 2F8h, 3E8h, 2E8h, or disabled. The serial ports are compatible with the serial-port implementation used on the IBM Serial Adapter. You can set the interrupts to INT3 - INT4. You can modify all base I/O-addresses and interrupts in the BIOS setup menu.

7.2 Signals

7.2.1 DTR#: Data Terminal Ready

This signal refers to the active-low, data-terminal ready outputs for the serial port. A handshake-output signal notifies the modem that the Universal Asynchronous Receiver/Transmitter (UART) is ready to establish a data-communication link.

7.2.2 RI#: Ring Indicator

This signal refers to the active-low input for the serial port. A handshake signal notifies the UART that the modem has detected a telephone ring signal.

7.2.3 TXD: Transmit Data

This signal refers to the transmitter serial-data output from the serial port.

7.2.4 RXD: Receive Data

This signal refers to the receiver serial-data input.

7.2.5 CTS#: Clear To Send

This signal refers to the active-low input for the serial port. A handshake signal notifies the UART that the modem is ready to receive data.

7.2.6 RTS#: Request To Send

This signal refers to the active-low output for the serial port. A handshake signal notifies the modem that the UART is ready to transmit data.

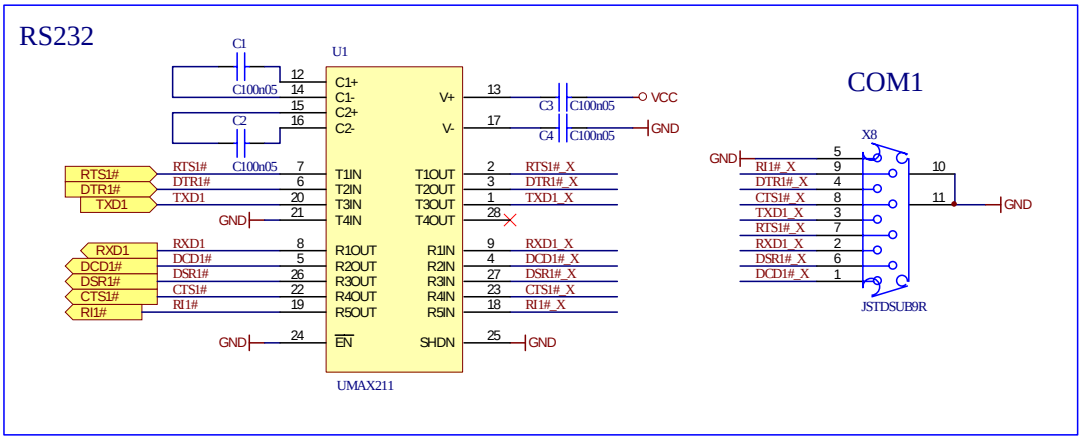
7.2.7 DCD#: Data Carrier Detect

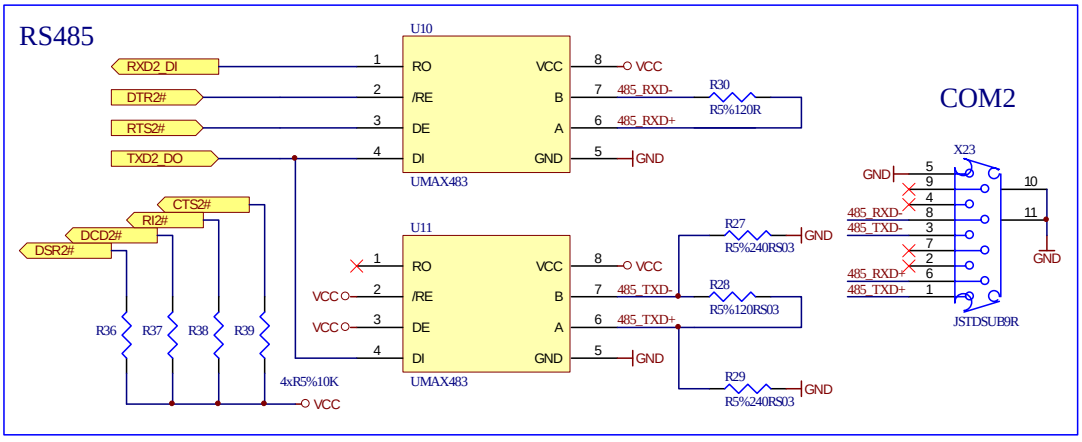
This signal refers to the active-low input for the serial port. A handshake signal notifies the UART that the modem has detected a carrier signal.

7.2.8 DSR#: Data Set Ready

This signal refers to the active-low input for the serial port. A handshake signal notifies the UART that the modem is ready to establish a communication link.

7.3 Design Example





8 Parallel Port Interface

The DIMM-PC/386-I/IE supports one parallel port (LPT1). This port maintains full compatibility with the PC/AT printer port and adds PS/2 bi-directional capability.

8.1 Configuration

The BIOS setup automatically configures the port. The parallel port's base I/O port address settings are 3BCh, 378h, 278h, or Disabled. The parallel-port mode settings are Normal and Extended. You can change the settings in the BIOS setup.

8.2 Signals

8.2.1 STB#: Strobe Signal

The active low pulse strobes the printer data into the printer.

8.2.2 AFD#: Autofeed Output

The active low output causes the printer to automatically feed one line after each line is printed.

8.2.3 PD [0-7]: Printer Data Bus

The bi-directional parallel data bus transfers information between the CPU and peripherals.

8.2.4 ERR#: Error

The active low signal indicates an error situation at the printer.

8.2.5 INIT#: Initiate Output

The active low signal initiates the printer when low.

8.2.6 SLIN#: Printer Select Input

The active low signal selects the printer.

8.2.7 ACK#: Acknowledge

The active low output from the printer indicates it has received the data and is ready to receive new data.

8.2.8 BUSY: Busy

The busy signal indicates the printer is busy and not ready to receive new data.

8.2.9 PE: Paper End

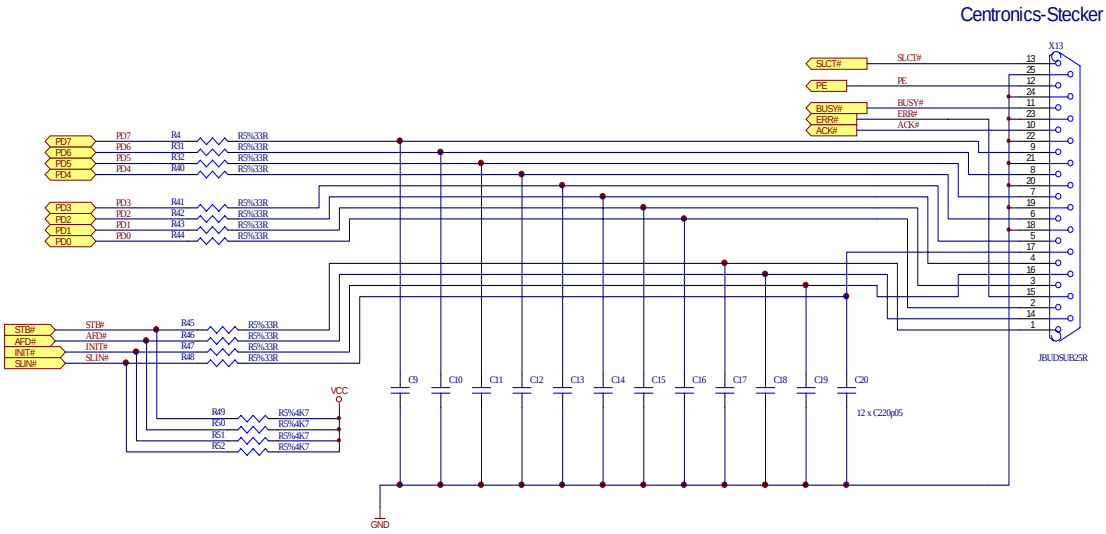
The PE signal indicates that the printer is out of paper.

8.2.10 SLCT: Printer Select Status

This active high output from the printer indicates that it has power on.

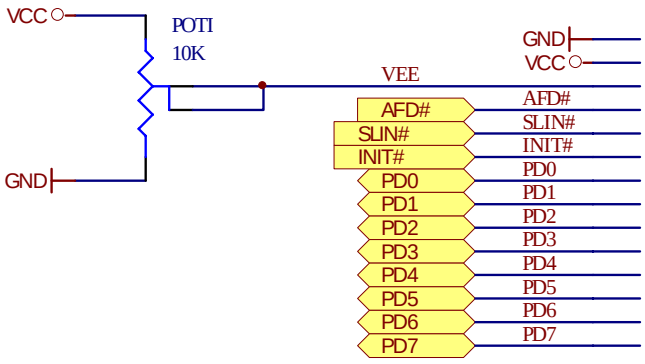
8.3 Design Example

8.3.1 Centronix Selector



8.3.2 Dot-Matrix Display

You can directly connect a standard dot-matrix display to the signals of printer port LPT1. For detailed pin descriptions, refer to the specifications from the manufacturer of the dot-matrix display.



Installing the Dot-Matrix Display

Turn on or reboot the system.

- ➤ Press <DEL> if asked to enter setup.
- ➤ Change the settings for the LPT Port to Extended Mode.
- ➤ Save the settings and then start DOS.
- ➤ Start the program D201LCD, which you can download from the Kontron Web site. If you use a display with two rows and 16 columns, the correct command line for the program is:

  D201LCD COPY 16 2 00 40 00 40
- ➤ Reboot. Display is now ready for use. The LCD driving voltage (contrast) can be changed by a Potentiometer.

Note: *You cannot use a dot-matrix display and a printer simultaneously. If you want to use a printer, enter the BIOS setup menu and change the settings for the LPT Port to normal.*

9 Keyboard Interface

The DIMM-PC/386-I/IE supports standard PC/AT style keyboards (AT and PS/2).

9.1 Configuration

BIOS configures the keyboard controller. The resources used by the keyboard controller are compatible with the PC/AT.

9.2 Signals

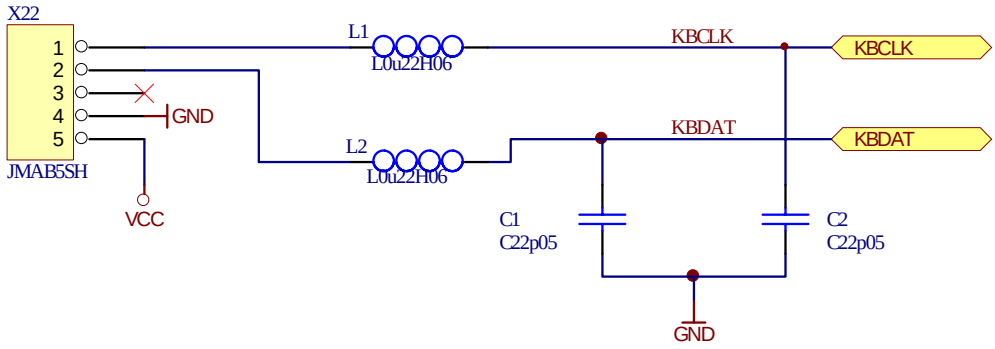
9.2.1 KBDAT: Keyboard Data

An open-collector output drives the bi-directional, keyboard-data signal.

9.2.2 KBCLK: Keyboard Clock

An open-collector output drives this keyboard-clock signal.

9.3 Design Example



10 Floppy Disk Interface

The floppy disk interface can support one drive. The drive may be 3.5" (720K, 1.44M, or 2.88M), or 5.25" (360K or 1.2M).

10.1 Configuration

The floppy disk controller (FDC) uses I/O, IRQ, and DMA resources. Configure the FDC in BIOS setup, choosing Disabled or Enabled. The resources used by the FDC are compatible with the PC/AT.

10.2 Signals

10.2.1 FDHDSEL#: Head Select

The active low output determines the active disk-drive head.

10.2.2 FDRDATA: Read Data

The active low, data-read signal from the disk is connected here.

10.2.3 FDWRPRT: Write Protect

The active low input senses from the disk drive that a disk is write-protected.

10.2.4 FDTRK0#: Track 0 Indicator

The active low input senses from the disk drive that the head is positioned over the outermost track.

10.2.5 FDWGATE#: Write Gate

The active low output enables the write circuitry of the disk drive.

10.2.6 FDWDATA#: Write Data

The active low output is a write, precompensated serial data that will be written on a selected disk drive.

10.2.7 FDSTEP#: Head Step Signal

The active-low output produces a pulse at a software-programmable rate to move the head during a seek operation.

10.2.8 FDDIR#: Head Step Direction

The active low output determines the direction of the head movement.

10.2.9 FDMTR0#: Motor Enable Signal

The active low output selects the motor of the disk drive.

10.2.10 FDDSKCHG#: Floppy Disk Change Signal

The disk-interface input indicates when the disk-drive door has been opened.

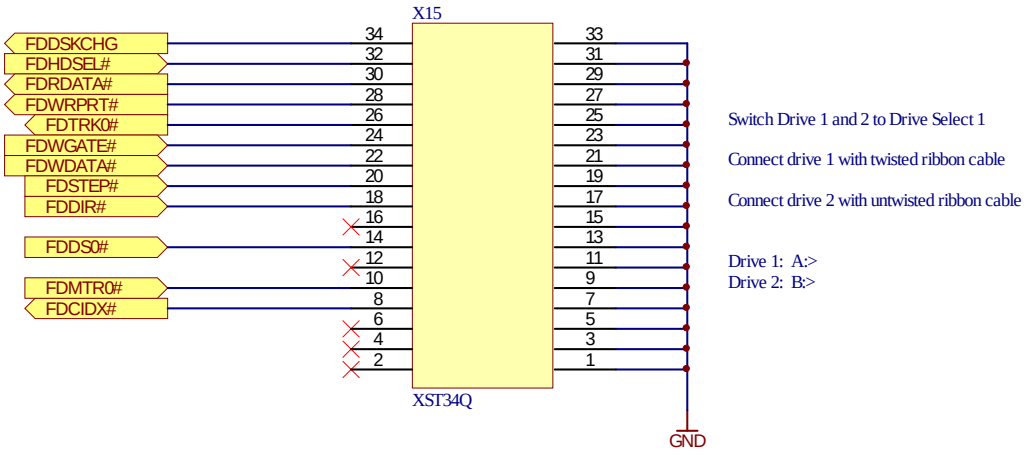
10.2.11 FDDS0#: Floppy Drive Select Signal

The active low output selects the disk drive.

10.2.12 FDCIDX#: Index Indicator

The active low input senses from the disk drive that the head is positioned over the beginning of a track, as marked by the index hole.

10.3 Design Example



11 IDE Hard Disk Interface

11.1 Configuration

Configure the external hard disk as the slave. Always configure the onboard IDE-compatible Flash hard disk as the master.

11.2 Signals

11.2.1 IDECS0#: IDE Chip Select 0

This hard disk chip select signal corresponds to the eight control-block addresses.

11.2.2 IDECS1#: IDE Chip Select 1

This hard disk chip select signal corresponds to the alternate status register.

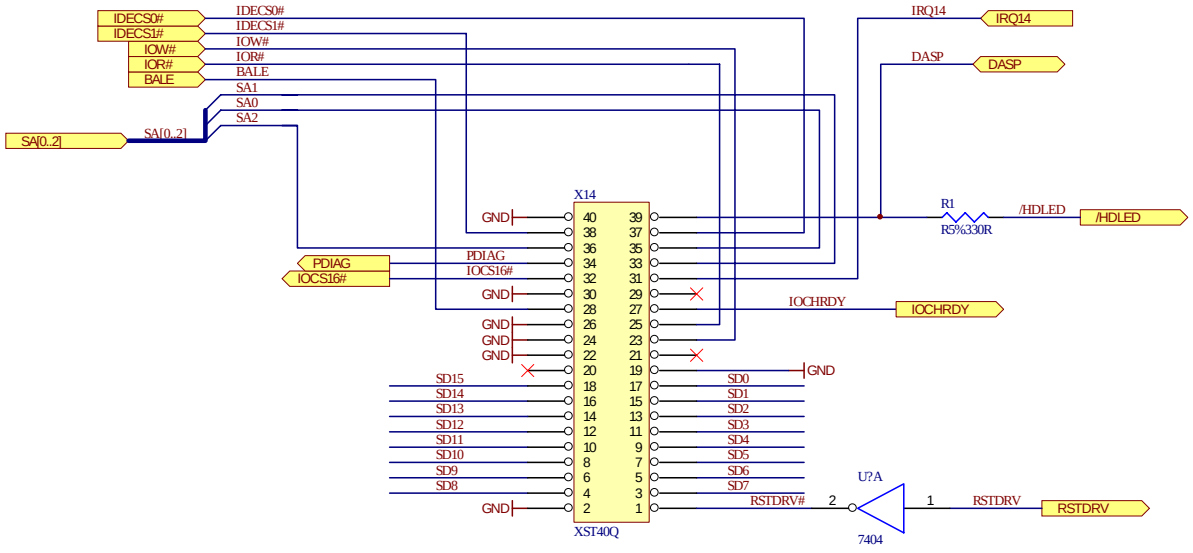
11.2.3 DASP

This time-multiplexed, open-collector, output signal indicates when a drive is active, or the presence of a slave drive. This signal is necessary for using IDE master/slave-mode on DIMM-PC/386-I/IE modules.

11.2.4 PDIAG

This signal is used as output by the drive if it is jumped in the slave mode or as input to the drive if it is jumped in the master mode. The signal indicates to a master that the slave has passed its internal diagnostic command. You must use the IDE master/slave-mode signal on DIMM-PC/386-I/IE modules.

11.3 Design Example



12 Ethernet Controller Interface

(DIMM-PC/386-IE only)

The Ethernet controller on the DIMM-PC/386-IE module consists of a CRYSTAL CS8900A from Cirrus Logic. The ISA Ethernet controller is a fully integrated 10BASE-T LAN solution.

12.1 Configuration

The Ethernet interface is an ISA device. The BIOS setup automatically configures it.

12.2 Signals

12.2.1 TXD+, TXD-: Transmit Signals

The differential output pair signals drive 10 MBps Manchester-encoded data to the 10BASE-T transmit lines.

12.2.2 RXD+, RXD-: Receive Signals

The differential input-pair signals receive 10 MBps of Manchester-encoded data from the 10BASE-T receive lines.

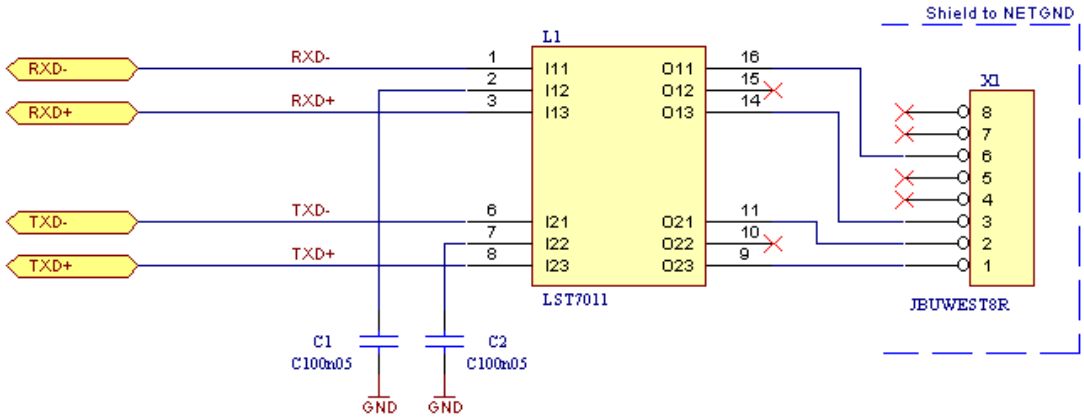
12.2.3 LNLED Status LED

The active low-output signal indicates transmission or reception of frames or detection of a collision. You can connect this to the external LED.

12.2.4 LKLED Status LED

This active low-output signal indicates valid 10BASE-T link pulses. You can connect this to the external LED.

12.3 Design Example



Parts Required to Connect to a 10BaseT Network

Quantity	Manufacturer	Order Number	Description
1	JAE	IL-Z- 4S-S125C3	Cable Socket for Ethernet Connector on DIMM-PC
4	JAE	IL-Z-C3-A-15000	Crimp Contacts (15000 pieces per reel)
1	Valor	ST7011	L1 (see above design example)
1	AMP	5-555178-3	X1 (see above design example)
2	Various	Unknown	Capacitors

13 Miscellaneous Interfaces

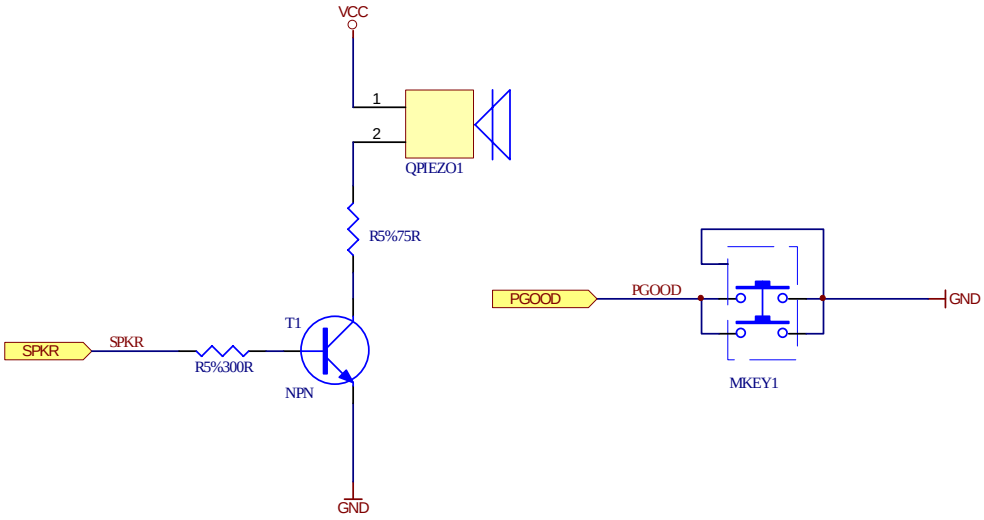
13.1 Speaker

You can connect an 8-Ohm loudspeaker between SPKR (Pin 134) and VCC (Pin 140).

13.1.1 SPKR: Speaker

Open the collector output on modules that drive a loudspeaker. An 8-Ohm loudspeaker connects between SPKR and VCC (+5V). Connect just one loudspeaker to this pin. The CPU typically drives this pin. However, other modules can use this signal to drive a system loudspeaker.

13.1.2 Design Example



13.2 Battery

The battery voltage has to be higher than 3.0V and lower than 4.0V. A 3V or 3.6V battery is recommended.

Note: *You do not need a battery to maintain CMOS setup data.*

13.2.1 BATT: System Battery Connection

This pin connects a system battery to all modules. The battery voltage has to be higher than 3.0V and lower than 4.0V. A 3V or 3.6V battery is recommended.

Because a capacitor supplies the RTC chip with power, you can disconnect the battery for at least an hour without losing time and setup information.

13.3 I2C-Bus

13.3.1 I2CLK: I2C-BUS CLK

The I2C-Bus Clock signal controls external I2C-bus slave devices.

13.3.2 I2DAT: I2C-BUS Data

The I2C-Bus Data signal controls external I2C-bus slave devices.

13.4 Power Good Reset

13.4.1 PGOOD Power Good

A high-active input for the DIMM CPU indicates that power from the power supply is ready. You also can use this as a low active-reset input signal.

13.5 Serial Interrupt Request

13.5.1 SMISW: SMI Interrupt Switch

This input generates the CPU's SMI interrupt.

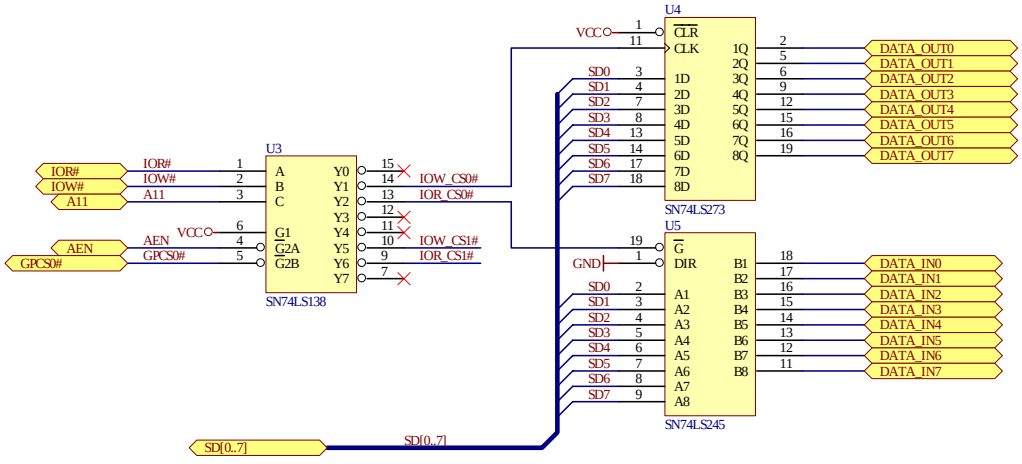
13.6 General Purpose Chip Select

The DIMM-PC/386-I/IE offers a programmable chip select output, which is available over the DIMM-PC bus.

13.6.1 GPCS0#: General Purpose Chip Select

The GPCS0# selects external peripherals. From the BIOS setup, you can change or disable the I/O-port address of the chip select.

13.6.2 Design Example



14 Watchdog Timer

The DIMM-PC/386-I/IE includes a Watchdog Timer (WDT) to ensure system integrity. When the WDT is triggered, it can generate a RESET or a NMI.

14.1 Configuration

From the BIOS setup, you can configure the WDT mode and timeout.

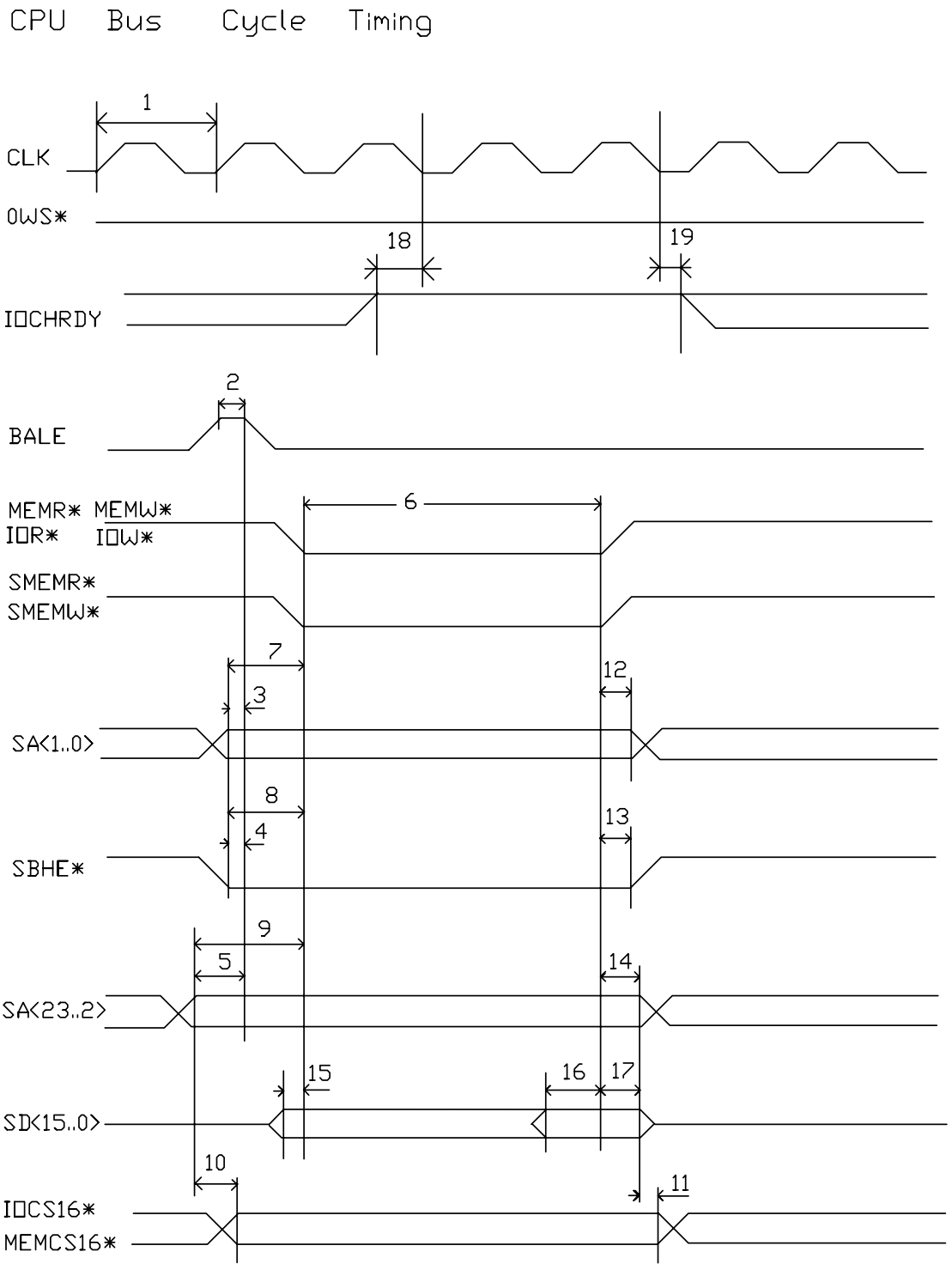
15 Timing Specifications

15.1 Bus

No.	Description	Min	Type	Max	Notes
1	Clock period (Tclk)	125			
2	BALE high width		54		
3	SA<1:0> setup to BALE low			8	
4	SBHE* setup to BALE low		20		
5	SA<23:2> setup to BALE low		130		
6a	Command width 16 bit cycles (zero wait states)		125		2
6b	Command with 8 bit cycles (with 2 wait states)		325		3
7	SA<1:0> setup to command zero cmd delay	8			1
8	SBHE* setup to command zero cmd delay		20		1
9	SA<23:2> setup to command zero cmd delay	130			1
10	MEMCS16*, IOCS16* delay from SA<23:2>			80	
11	MEMCS16*, IOCS16* hold after SA<23:2	0			
12a	SA<1:0> hold after command	23			
12b	SA<1:0> hold after SMEMR* or SMEMW*		18		
13a	SBHE* hold after command	23			
13b	SBHE* hold after SMEMR* or SMEMW*	18			
14a	SA<23:2> hold after command	30			
14b	SA<23:2> hold after SMEMR* or SMEMW*	25			
15	Write Data setup to command active		6		
16	Read Data setup to command inactive	65			1
17a	Write Data hold after command	45			
17b	Read Data hold after command	0			
18	IOCHRDY setup to CLK	34			
19	IOCHRDY hold after CLK	2			
20	0WS* setup to CLK	20			
21	0WS* hold after CLK	0			

Notes: *[1] Command delay programmable between 0 and 3 CLK/2 cycles separately for 16-bit memory, 8-bit memory and I/O cycles.*
[2] Command width depends on the number of wait states (programmable from 0 to 3 CLK cycles) and command delay.
[3] Command width depends on the number of wait states (programmable from 2 to 5 CLK cycles) and command delay.

15.1.1 Timing Diagram



15.2 DMA

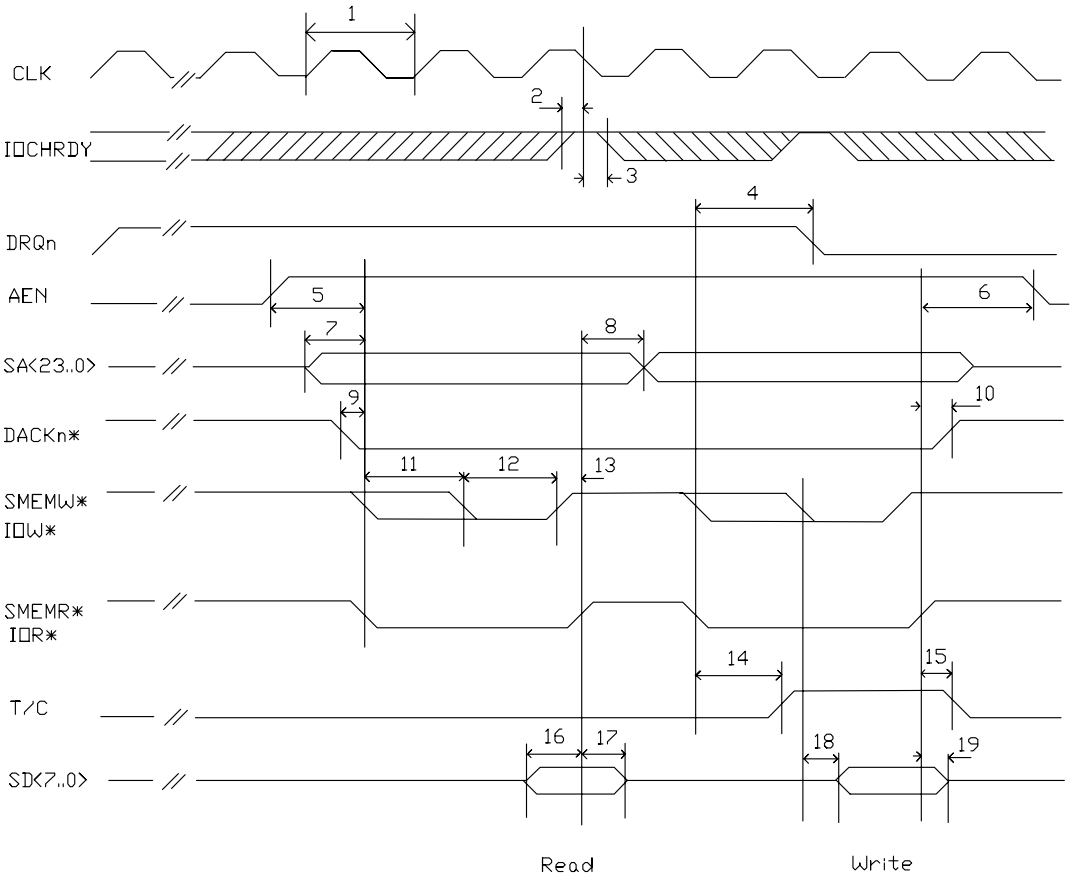
The table specifies timing for DMA cycles in ns.

No.	Description	Min	Type	Max	Note
1	Clock period (Tclk)	125			
2	IOCHRDY setup to CLK	35			
3	IOCHRDY hold from CLK	20			
4	DRQ inactive delay from command			55	
5	AEN setup to command	80			
6	AEN hold from command	10			
7	SA<23:0> setup to command	50			
8	SA<23:0> hold from command	50			
9	DACK setup to command	0			
10	DACK hold from command		0		
11	Extended Write delay	122		128	
12	Write command width (Extended Write , 0 Wait states)	80			1
13	Read inactive delay from Write	20			
14	T/C delay from command			165	
15	T/C hold from command	0			
16	Read data setup	110			
17	Read data hold	0			
18	Write data delay after command			80	2
19	Write data hold	15			

Notes: *[1] With programmable wait states from 1 to 4 CLK cycles.*
[2] This time cannot be extended by insertion of wait states.

15.2.1 Timing Diagram

DMA – Timing

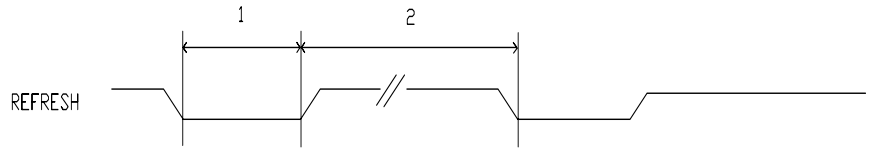


15.3 Refresh

No.	Description	Min
1	REFRESH pulse width	750ns
2	REFRESH inactive time	15,6µS

15.3.1 Timing Diagram

REFRESH Signal Timing



16 Appendix A: System Resources

16.1 Interrupt Request Lines

IRQ #	Used for	Available
0	Timer0	No
1	Keyboard	No
2	Slave 8259	No
3	COM2	Note (1)
4	COM1	Note (1)
5	LPT2	Yes
6	FDC	Note (1)
7	LPT1	Note (1)
8	RTC	No
9		Yes
10	Ethernet	Available if a board without Ethernet is used Note(2)
11		Yes
12		Yes
13		No
14	IDE0	Note (1)
15		Yes

Note: *[1] If the "Used for" device is disabled in setup, the corresponding interrupt is available for other devices.*
[2] Available if a module without Ethernet is used (DIMM-PC/386-I).

16.2 Direct Memory Access Channels

DMA #	Used For	Available	Comment
0		Yes	
1		No	Not on DIMM-PC bus
2	FDC	No	Available if disabled
3	LPT	No	Not on DIMM-PC bus
4	Cascade	No	
5		Yes	
6		No	Not on DIMM-PC bus
7	Ethernet	No	Available if board does not have Ethernet

16.3 Upper Memory Area Map

Upper Memory	Used For	Available
A0000h – BFFFFh		Yes
C0000h – DFFFFh		Yes BIOS at C0000 is assumed to be VGA
E0000h – F0000h	System BIOS	No

16.4 I²C Bus

I2C Address	Used For	Available
A0h	EEPROM	No
B0h	reserved	No
58h	reserved	No

16.5 DIMM-PC Bus Connector Pin Out

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	IOCHCK#	2	GND	3	RSTDRV
4	IDECS0#	5	SD7	6	VCC
7	SD6	8	IDECS1#	9	IRQ9
10	DASP	11	SD5	12	PDIAG
13	SD4	14	DTR2#	15	DRQ2
16	RI2#	17	SD3	18	TXD2
19	SD2	20	CTS2#	21	MEMCS16#
22	RXD2	23	SD1	24	RTS2#
25	0WS#	26	DCD2#	27	IOCS16#
28	GND	29	SD0	30	DSR2#
31	SBHE#	32	FDHDSEL#	33	IOCHRDY
34	FDRDATA#	35	IRQ10	36	FDWRPRT#
37	AEN	38	FDTRK0#	39	SMEMW#
40	FDWGATE#	41	IRQ11	42	FDWDATA#
43	SA19	44	FDSTEP#	45	SMEMR#
46	FDDIR#	47	IRQ12	48	FDMTR0#
49	SA18	50	FDDSKCHG	51	IOW#
52	FDDS0#	53	IRQ15	54	FDIDX#
55	SA17	56	USB1- (*)	57	IOR#
58	GND	59	IRQ14	60	SA16
61	DACK0#	62	GND	63	SA15
64	USB1+ (*)	65	DRQ0	66	VCC
67	SA14	68	LNLED	69	DACK5#
70	LKLED	71	SA13	72	I2CDAT
73	DRQ5	74	I2CCLK	75	SA12
76	GPCS0#	77	REF#	78	DCD1#
79	SD8	80	DSR1#	81	SA11
82	RXD1	83	SYSCLK	84	RTS1#
85	SD9	86	TXD1	87	SA10
88	CTS1#	89	IRQ7	90	GND
91	SD10	92	DTR1#	93	SA9
94	RI1#	95	IRQ6	96	STB#
97	SD11	98	AFD#	99	SA8
100	PD0	101	IRQ5	102	ERR#
103	SD12	104	PD1	105	SA7
106	INIT#	107	IRQ4	108	PD2
109	DACK7#	110	SLIN#	111	DRQ7
112	PD3	113	IRQ3	114	PD4
115	SA6	116	PD5	117	SD13
118	PD6	119	DACK2#	120	PD7
121	SA5	122	ACK#	123	SD14
124	BUSY	125	TC	126	PE
127	SA4	128	SLCT#	129	SD15
130	KBDAT	131	BALE	132	KBCLK
133	SA3	134	SPKR	135	MASTER#
136	PGOOD	137	SA2	138	SMISW
139	SA1	140	VCC	141	OSC
142	BATT	143	SA0	144	GND

Note: *(*) Not available on the DIMM-PC/386-I/IE.*

16.6 I/O Map

The I/O port addresses of the processor module DIMM-PC are functionally identical to a standard PC/AT.

I/O Addresses	DIMM-PC/386-I/IE	Function
0000 - 001F	x	DMA Controller 1
0020 - 003F	x	Interrupt Controller 1
0040 - 0043	x	Timer
0050 - 005F	x	Onboard Control Registers
0060 - 0064	x	Keyboard Controller
0061	x	Port B Register
0070	x	NMI Enable Register
0070 - 0071	x	Real Time Clock
0080 - 008F	x	DMA Page Register 74LS612
0092	x	Port A Register (Fast A20 Gate)
00A0 - 00BF	x	Interrupt Controller 2
00C0 - 00DF	x	DMA Controller 2
00F0 - 00FF		Math Coprocessor
0100		I/O Channel
0110	x	General Purpose Chip Select
01F0 - 01F7	x	Fixed Disk
0200 – 0207		Game I/O
020C-020D		Reserved
021F		Reserved
0220	x	General Purpose Chip Select
0278 - 027F		Parallel Port 2
02B0 - 02DF		Alternate Enhanced Graphics Adapter
02E1		GPIB (Adapter 0)
02E2 - 02E3		Data acquisition (Adapter 0)
02F8 - 02FF	x	Serial Port 2
0300 - 030F		Onboard Network (default configuration)
0310 - 031F		Prototype Card
0330	x	General Purpose Chip Select
0360 – 0363		PC Network (low address)
0364 – 0367		Reserved
0368 - 036B		PC Network (high address)
036C - 036F		Reserved
0378 - 037F	x	Parallel Port 1
0380 - 038F		SDLC, Bisynchronous 2
0390 – 0393		Cluster
03A0 - 03AF		Bisynchronous 1
03B0 - 03BF		Monochrome Display and Printer Adapter
03C0 - 03CF		Enhanced Graphic Adapter
03D0 - 03DF		Color/Graphic Monitor Adapter
03F0 - 03F7	x	Diskette Controller
03F8 - 03FF	x	Serial Port 1

17 Appendix B: BIOS Operation

The standard AMIBIOS is located in the onboard Flash memory. This device has an 8-bit wide access. The 16-bit access is enabled by the shadow-RAM feature (standard). The extended BIOS for special ***DIMM-PC/386-I/IE*** features also is located in the Flash memory.

Note: *The Extended BIOS uses Memory Segment E. Disable this segment to use EMM386 (X=E000-FFFF).*

17.1 Setup Utility

The setup utility configures system information that is stored in NVRAM. Press the **<DEL>** key during the Power-On-Self-Test (POST) to start the setup utility after the following message appears:

```
Hit <DEL> if you want to run SETUP
```

17.1.1 Help Screens

Choose **Help** by pressing **<Alt> <H>.** Press **<Esc>** to exit **Help**.

17.1.2 Automatic Setup Utility Option Selection

If selecting a setting for one setup utility option determines the settings for one or more other setup utility options, AMIBIOS assigns the dependent settings and does not permit you to modify the settings unless the setting for the parent option has been changed.

For example, you can set serial-port options in the **Peripheral Setup** to *2F8h*, *3F8h*, *2E8h*, or *3E8h*. If *2F8h* is chosen for Serial Port 1, AMIBIOS disables *2F8h* for Serial Port 2. Invalid options are grayed and cannot be selected.

17.1.3 Using the Keyboard

The setup utility has a built-in keyboard driver that uses simple keystroke combinations:

Keystroke	Function
<Tab>	Move to the next window or field.
→,←,↑,↓	Move to the next field to the right, left, above, or below.
<Enter>	Select in the current field.
+	Increments a value.
-	Decrements a value.
<Esc>	Close current operation and return to previous level.
<PgUp>	Return to previous page.
<PgDn>	Advance to next page.
<Home>	Return to beginning of the text.
<End>	Advance to end of the text.
<Alt> <H>	Access a help window.
<Alt> <Spacebar>	Exit setup utility.
Alphabetic keys	A to Z are used in the virtual keyboard and are not case-sensitive.
Numeric keys	0 to 9 are used in the virtual keyboard and numeric keypad.

17.2 Main Menu

The main menu of the **Setup Utility** is organized into four windows. Each window corresponds to a section in this chapter. Each section contains several icons. Clicking an icon activates a function.

Setup-utility icons and functions are described in this chapter. Sections include:

Windows	Function
Setup	This section has tree icons that permit you to set system configuration options such as date, time, hard-disk type, floppy type, and others.
Utility	This section has two icons that perform system functions.
Security	This section has one icon that controls AMIBIOS security features.
Default	This section has three icons that permit you to select a group of settings for all setup utility options.

17.3 Setup Window

The **Setup Window** utility has six screens. Different system-configuration parameters are set on each screen.

Type	Description
Standard setup	Sets time and date. Configures disk drives.
Advanced setup	Configures performance parameters.
Peripheral setup	Configures I/O support.

17.4 Standard Setup

You can display Standard setup options by choosing the **Standard** icon from the setup utility menu. Standard setup options include.

17.4.1 Date/Time

Select the Date/Time option to change the date or time. The current date and time are displayed. Enter new values using the displayed window.

17.4.2 Floppy Drive

Choose the Floppy Drive A or B icon to specify the drive type. Settings include *360 KB 5¼"*, *1.2 MB 5¼"*, *720 KB 3½"*, *1.44 MB 3½"*, or *2.88 MB 3½"*.

17.4.3 Master Disk / Slave Disk

Choose these icons to configure the hard-disk drive named in the option. All parameters relate to IDE drives except **Type.**

17.4.4 Configuring an MFM Drive

If configuring an MFM hard-disk drive, you must know the drive parameters (number of heads, number of cylinders, number of sectors, the starting write precompensation cylinder, and drive capacity). Choose **Type** and choose the appropriate hard disk drive type (1-46). The old MFM hard-drive types are listed on

Pages 39-40. If the drive parameters of your MFM drive do not match a drive type on page 39-40, select *User* in the **Type** field and enter the drive parameters on the screen that appears.

17.4.5 User-Defined Drive

If you are configuring a SCSI drive or an MFM, RLL, ARLL, or ESDI drive with drive parameters that do not match drive types 1-46, you can select the *User* in the **Type** field. Enter the drive parameters on the screen. Drive parameters include:

- Cylinder (number of cylinders)
- Hd (number of heads)
- WP (starting write precompensation cylinder)
- Sec (number of sectors)
- Size (drive capacity)

Parameter	Description
Type	The number for a drive with certain identification parameters.
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.
Write Precompensation	The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number in which write precompensation begins.
Landing Zone	This number is the cylinder location in which heads normally park when the system is shut down.
Sectors	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drives have more sectors per track.
Capacity	The formatted capacity of the drive is (Number of heads) x (Number of cylinders) x (Number of sectors per track) x (512 bytes per sector)

17.4.6 Configuring IDE Drives

When configuring an IDE drive, select the appropriate drive icon (*Pri Master* or *Pri Slave*). Select the **IDE Setup** icon to detect drive parameters. AMIBIOS detects the IDE drive and displays them. Click **OK** to accept the parameters. Or, set the parameters if you know the correct ones.

DIMM-PC/386-I/IE has an onboard IDE-compatible Flash hard disk, which you must configure as Master. If you connect external IDE drives, jumper the external drive as slave.

17.4.7 Hard Disk Drive Types

Type	Cylinders	Heads	Write Precompensation	Landing Zone	Sectors	Capacity
1	306	4	128	305	17	10 MB
2	615	4	300	615	17	20 MB
3	615	6	300	615	17	31 MB
4	940	8	512	940	17	62 MB
5	940	6	512	940	17	47 MB
6	615	4	65535	615	17	20 MB
7	462	8	256	511	17	31 MB
8	733	5	65535	733	17	30 MB
9	900	15	65535	901	17	112 MB
10	820	3	65535	820	17	20 MB
11	855	5	65535	855	17	35 MB
12	855	7	65535	855	17	50 MB
13	306	8	128	319	17	20 MB
14	733	7	65535	733	17	43 MB
16	612	4	0	663	17	20 MB
17	977	5	300	977	17	41 MB
18	977	7	65535	977	17	57 MB
19	1024	7	512	1023	17	60 MB
20	733	5	300	732	17	30 MB
21	733	7	300	732	17	43 MB
22	733	5	300	733	17	30 MB
23	306	4	0	336	17	10 MB
24	925	7	0	925	17	54 MB
25	925	9	65535	925	17	69 MB
26	754	7	754	754	17	44 MB
27	754	11	65535	754	17	69 MB
28	699	7	256	699	17	41 MB
29	823	10	65535	823	17	68 MB
30	918	7	918	918	17	53 MB
31	1024	11	65535	1024	17	94 MB
32	1024	15	65535	1024	17	128 MB
33	1024	5	1024	1024	17	43 MB
34	612	2	128	612	17	10 MB
35	1024	9	65535	1024	17	77 MB
36	1024	8	512	1024	17	68 MB
37	615	8	128	615	17	41 MB
38	987	3	987	987	17	25 MB
39	987	7	987	987	17	57 MB
40	820	6	820	820	17	41 MB
41	977	5	977	977	17	41 MB
42	981	5	981	981	17	41 MB
43	830	7	512	830	17	48 MB
44	830	10	65535	830	17	69 MB
45	917	15	65535	918	17	114 MB
46	1224	15	65535	1223	17	152 MB
USER		USER-DEFINED HARD DRIVE - Enter user-supplied parameters.				

17.5 Advanced Setup

Choosing the **Advanced** icon displays advanced setup options from the Setup utility main menu. The available advanced setup options are described below.

17.5.1 Typematic Rate

This option specifies the speed at which a keyboard keystroke repeats. The settings are *Default, 15, 20* or *30*.

17.5.2 System Keyboard

This option specifies that a keyboard is attached to the computer. The settings are *Present* or *Absent*. The Optimal and Fail-Safe default settings are *Absent*.

17.5.3 Primary Display

This option specifies the type of display monitor and adapter in the computer. The settings are *Absent, VGA/EGA, CGA40x25, CGA80x25* and *Mono*. The Optimal and Fail-Safe default settings are *Absent*.

17.5.4 Above 1 MB Memory Test

Set option to *Disabled* to instruct AMIBIOS to boot quickly when the computer is powered on. The Optimal and Fail-Safe default settings are *Disabled*.

17.5.5 Memory Test Tick Sound

Set option to *Enabled* to instruct AMIBIOS to boot with Tick when the computer is testing memory. The Optimal and Fail-Safe default settings are *Enabled*.

17.5.6 Parity Error Check

Set option to *Enabled* to check parity. This option enables NMI for IOCHCK-Error on ISA-Bus. The settings are *Disabled* or *Enabled*. The Optimal and Fail-Safe default settings are *Disabled*.

17.5.7 Hit Del Message Display

Set this option to *Disabled* to prevent

Hit <DEL> if you want to run Setup

17.5.8 Extended BIOS RAM Area

The settings are *0:300* or *DOS 1k*.

17.5.9 Wait for F1 if Error

AMIBIOS POST error messages are followed by:

Press <F1> to continue

If this option is set to *Disabled,* AMIBIOS does not wait for you to press the **<F1>** key after an error message. The settings are *Disabled* or *Enabled*. The Optimal and Fail-Safe default settings are *Disabled*.

17.5.10 Boot Up Num Lock

Set this option to *Off* to turn the **Num Lock** key off when the computer is booted so you can use the arrow keys on the numeric keypad and the keyboard. The settings are *On* or *Off*. The default settings are *On*.

17.5.11 Floppy Drive Seek

Set this option to *Enabled* to specify that floppy drive A will perform a seek operation at system boot. The settings are *Disabled* or *Enabled*. The Optimal and Fail-Safe default settings are *Disabled*.

17.5.12 Boot Up Sequence

This option sets the sequence of boot drives (Floppy drive A:, Hard-disk drive C:) that the AMIBIOS attempts to boot from after AMIBIOS POST completes. The settings are *C:,A:* or *A:,C:*.

17.5.13 Password Check

This option enables password checking every time the computer powers on or every time the setup utility executes. If *Always* is chosen, a user password prompt appears when the computer is turned on. If *Setup* is chosen, the password prompt appears if the setup utility is executed. The Optimal and Power-On defaults are *Setup*.

17.5.14 Video

Options include:

- Shadow C000,32K
- Shadow C800,32K
- Shadow D000,32K
- Shadow D800,32K

The options control the location of the contents of the 32KB of ROM, beginning at the specified memory location. If no adapter ROM uses the named ROM area, this area is made available to the local bus. The settings are:

Setting	Description
Enable	The contents of the 32K area starting at xx000h are written to the same address in system memory (RAM) for faster execution.
Disabled	The ROM is not copied to RAM. The contents of the ROM cannot be read from or written to memory.

17.6 IDE Options

17.6.1 Primary IDE 32 Bit Transfer

Set this option to *Enabled* to support IDE drives that permit 32-bit accesses. The settings are *Disabled* or *Enabled*. The Optimal and Fail-Safe default settings are *Disabled*.

17.6.2 Primary IDE Block Mode

Set this option to *Enabled* to support IDE drives that use Block Mode. The settings are *Disabled* or *Enabled*. The Optimal and Fail-Safe default settings are *Disabled*.

17.6.3 Primary IDE LBA Mode

Set this option to *Enabled* to support IDE drives with capacities greater than 528 MB. The settings are *Disabled* or *Enabled*. The Optimal and Fail-Safe default settings are *Disabled*.

17.6.4 IDE HDD Auto Detection

If this option is set to *Enabled*, the BIOS detects IDE drive parameters. The settings are *Disabled* or *Enabled*. The Optimal and Fail-Safe default settings are *Disabled*.

17.7 Special Options

17.7.1 Watchdog Mode

Set this option to support the watchdog on DIMM-PC/386-I/IE. The settings are *Disabled*, *RESET* and *NMI*. If you set the option to *RESET*, the watchdog will generate a system reset and option NMI will generate a nonmaskable interrupt after the watchdog times out.

17.7.2 Watchdog Timeout

This option changes the timeout, which triggers Watchdog. Settings are *0.4sec, 1sec, 5sec, 10sec, 30sec, 1min, 5min*, and *8.5min*.

17.7.3 GPCS Address

Set this option to change the I/O port address of the General Purpose Chip Select, which connects to the DIMM-PC bus and is available for external application. Settings include *disabled, 110h, 220h or 330h*. The Optimal and Fail-Safe default settings are *Disabled*.

17.7.4 CPU Clock

Set this option to change the clock speed of the CPU from 10 to 40 MHz. The MHz settings are *10, 12, 16, 25, 30, 33* and *40*. Optimal and Fail-Safe default settings are *33 MHz*.

17.7.5 Reserved Memory Size

Set this option to provide a given sum of memory that will be not used while the system boots up. The settings are *Disabled*, *32K,* and *64K*.

17.7.6 Reserved Memory Address

Set option to select position of reserved memory area. Settings are *C800*, *D000* and *D800*.

17.8 Peripheral Setup

Peripheral setup options are displayed by choosing the Peripheral Setup icon from the setup utility menu. Peripheral setup options are described in this section.

17.8.1 Onboard FDC

This option enables the floppy-drive controller on the motherboard. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Enabled*.

17.8.2 Onboard IDE

This option enables the IDE controller on the motherboard. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Enabled*.

17.8.3 Onboard Serial Port1

This option enables Serial Port 1 on the motherboard and specifies the base I/O port address for Serial Port 1. The settings are *3F8h, 2F8h, 3E8h, 2E8h* or *Disabled*. The Optimal and Fail-Safe default settings are *3F8h*.

17.8.4 Onboard Serial Port2

This option enables Serial Port 2 on the motherboard and specifies the base I/O port address for Serial Port 2. The settings are *3F8h, 2F8h, 3E8h, 2E8h* or *Disabled*. The Optimal and Fail-Safe default settings are *2F8h*.

17.8.5 Onboard Parallel Port

This option enables the parallel port on the motherboard and specifies the parallel-port base, I/O-port address. The settings are *3BCh, 378h, 278h,* or *Disabled*. The Optimal and Fail-Safe default setting are *378h*.

17.8.6 Parallel Port Mode

This option specifies the parallel-port mode. The settings are *Normal* and *Extended*. The Optimal and Fail-Safe default setting are *Extended*.

17.9 Utility

The following icons appear in this section of the Setup utility main screen.

17.9.1 Color Set

This feature sets the Setup screen colors. Settings are *LCD, Army, Pastel* and *Sky*.

17.9.2 IDE Setup

This feature detects the IDE drive and displays it. Click **OK** to accept the parameters. IDE detection always locates the onboard IDE-compatible flash hard disk as master and then selects the optional connected external hard disk, which must be configured as slave.

17.10 Security

One icon appears in this part of the setup utility screen.

17.10.1 Password

You can configure the system so that all users must enter a password when the system boots or when the setup utility executes.

17.10.2 Setting a Password

The password check option is enabled in **Advanced**. By choosing *Always* (the password prompt appears when the system is powered on) or *Setup* (the password prompt appears only when the Setup utility is started). The password is encrypted and stored in NVRAM.

If you do not want to use a password, press <**Enter**> when the password prompt appears.

17.10.3 Changing a Password

Select the *Password* setting from the **Security** section of the setup menu. Enter the password in the **Security** section and press <**Enter**>. The screen does not display the characters entered. After entering the new password, retype the new password as prompted and press <**Enter**>.

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press <**Esc**>. The password is stored in NVRAM after the setup utility completes. The next time the system boots, a password prompt appears.

Remember the Password

Keep a record of the new password when the password changes. If you forget the password, erase the system configuration information in NVRAM. Default

The icons in this section permit you to select a group of settings for all setup- utility options. Use these icons to set system-configuration parameters and choose a group of settings that have a better chance of working when the system experiences configuration-related problems.

17.11 Default

17.11.1 Original

Choose the **Original** icon to return to the system configuration values present in setup utility.

17.11.2 Optimal

You can load the optimal default settings for the setup utility by selecting the **Optimal** icon. Optimal default settings are best-case values that should optimize performance.

17.11.3 Fail-Safe

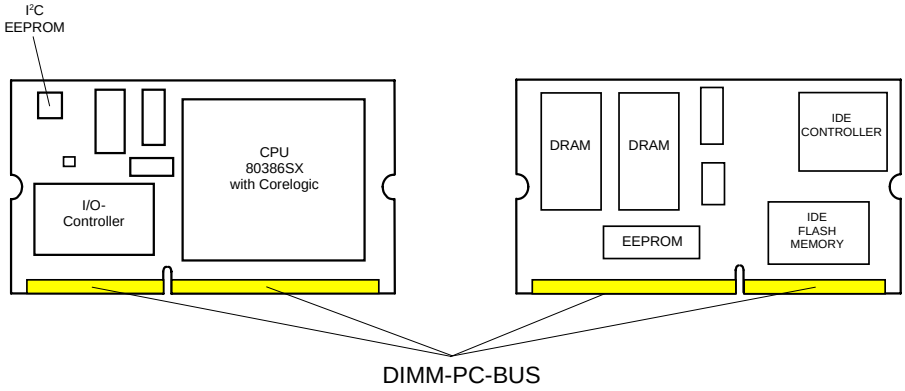
You can load the Fail-Safe, setup-option settings by selecting the Fail-Safe icon from the Default section of the setup menu.

Fail-Safe settings do not provide optimal system performance but are the most stable settings. Use this option as a diagnostic aid if the system behaves erratically.

If the NVRAM is corrupted, the Fail-Safe settings automatically load.

18 Appendix C: Connectors

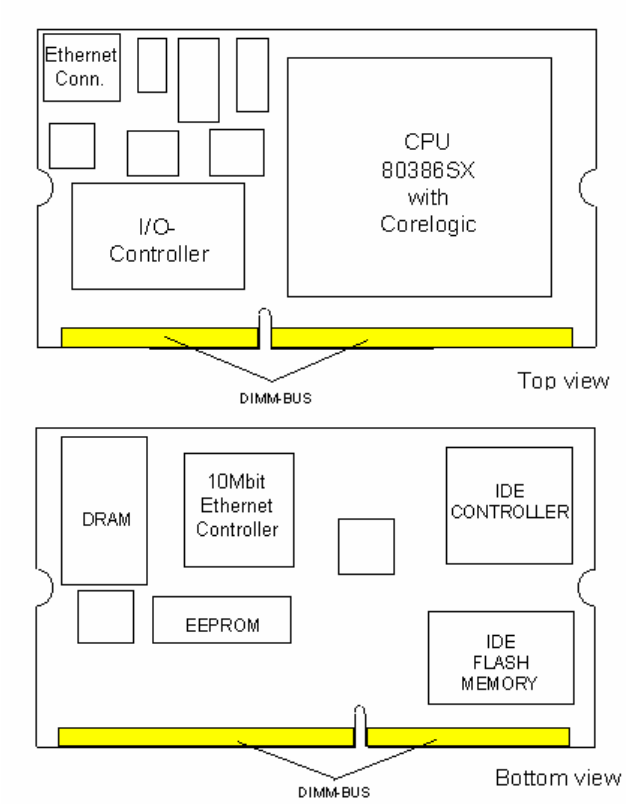
18.1 DIMM-PC 386-I Bus



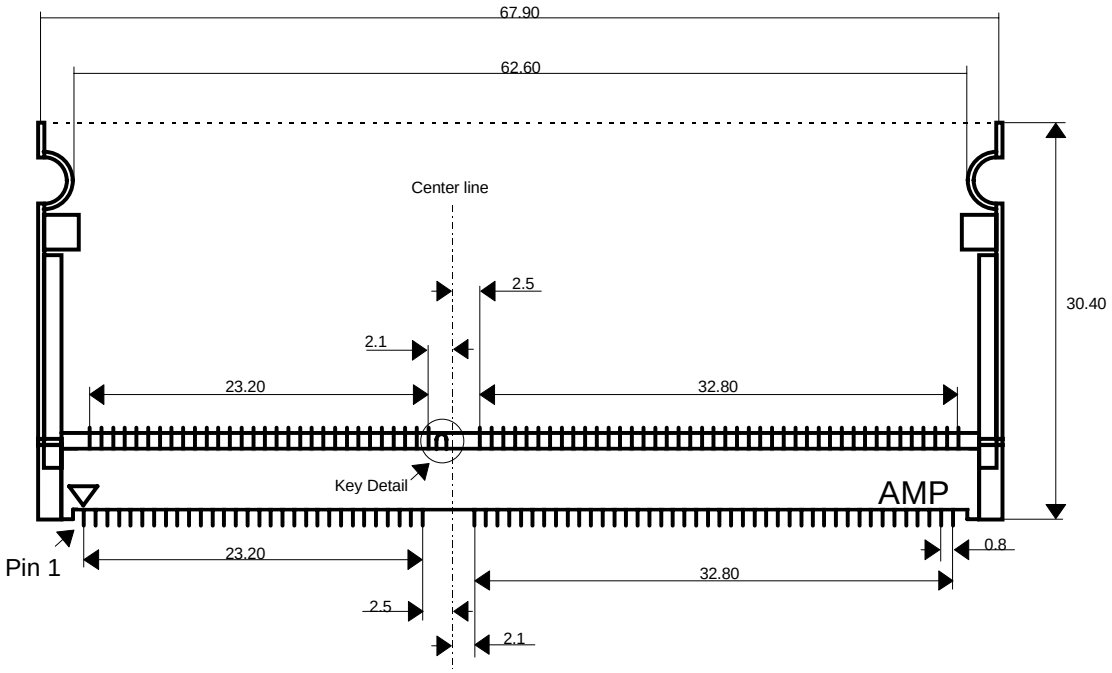
Top view Bottom view

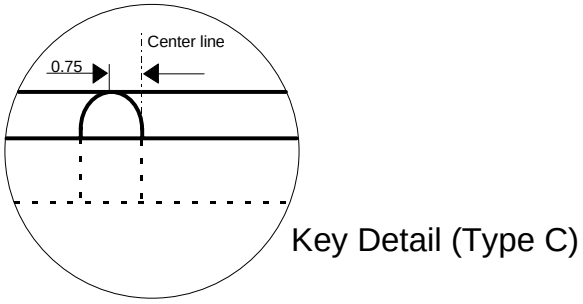
18.2 DIMM-PC 386-IE Bus

The Ethernet controller is only available on DIMM-PC/386-IE.

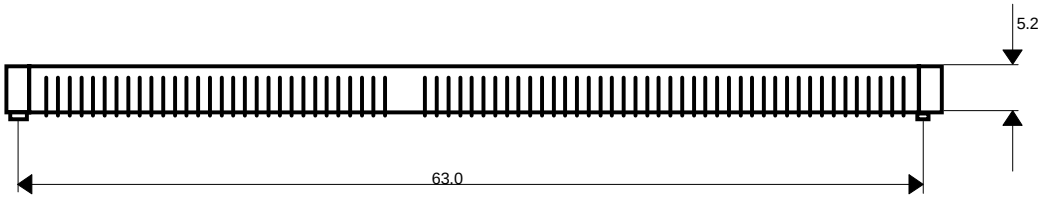


18.3 Mating Socket



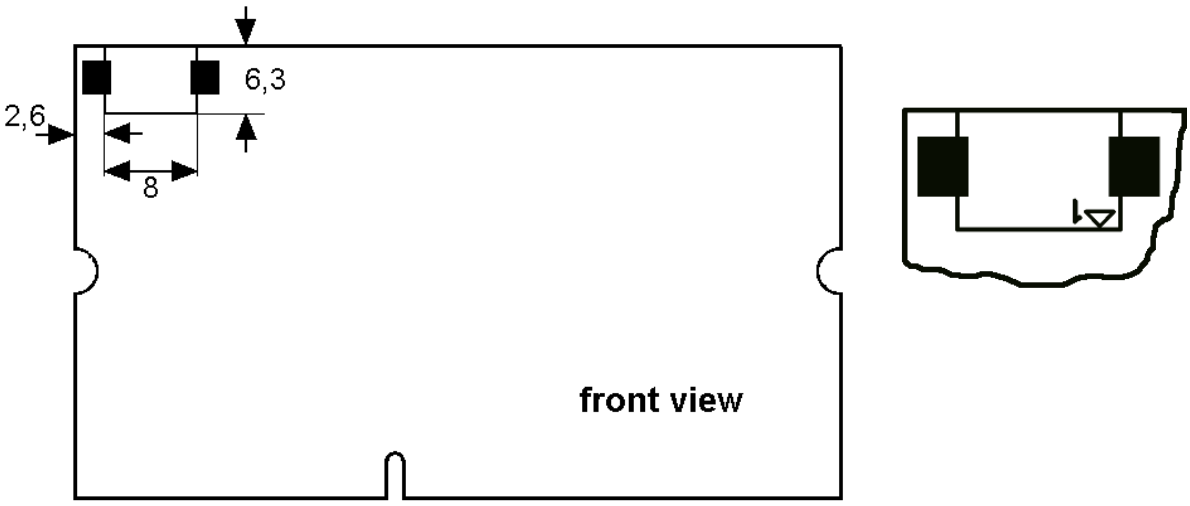


Key Detail (Type C)



18.4 Ethernet

The Ethernet controller is only available on DIMM-PC/386-IE.

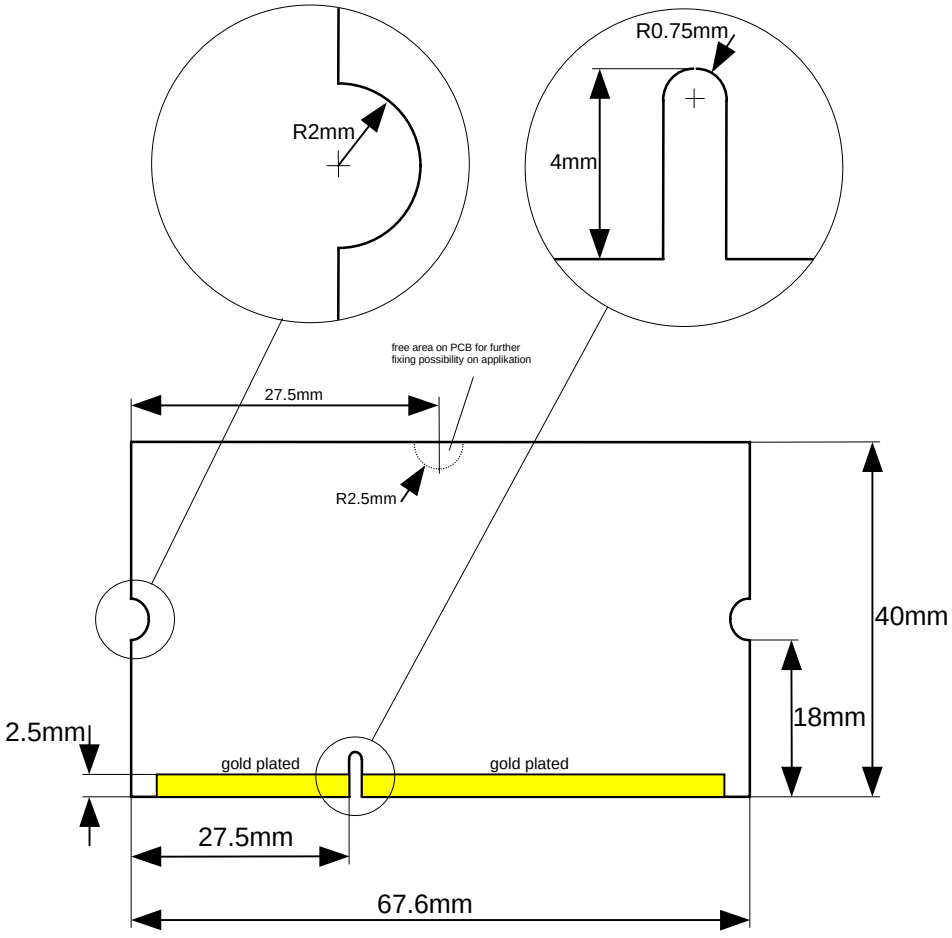


18.4.1 Supply Voltage

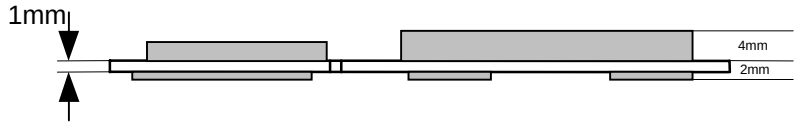
Pin Number	Signal
1	TXD+
2	TXD-
3	RXD+
4	RXD-

19 Appendix D: Mechanical Dimensions

19.1 Front and Side View



front view

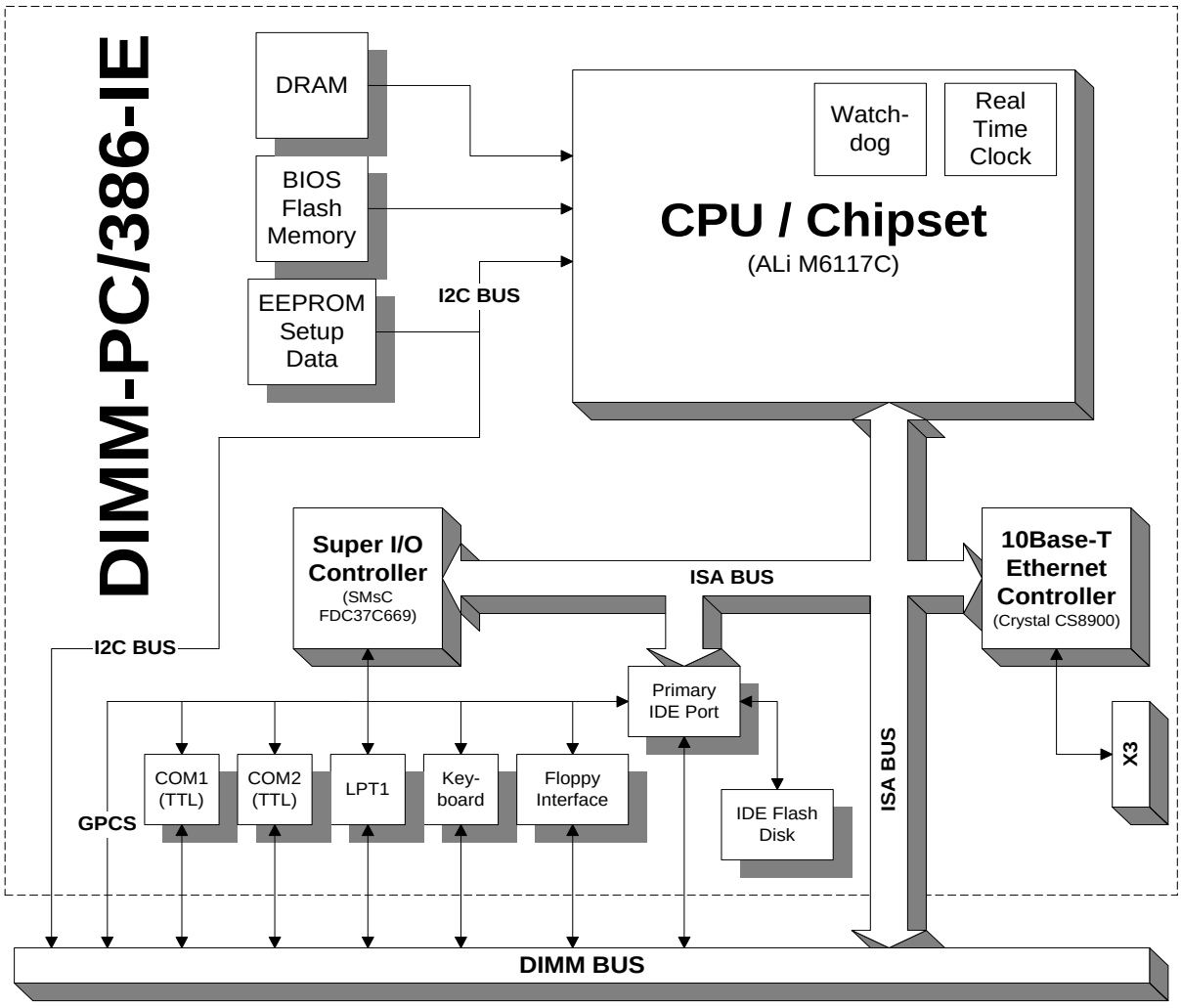


side view

20 Appendix E: Block Diagrams

20.1 DIMM-PC/386-I/IE

(Ethernet feature is only available on DIMM-PC/386-IE variants).



21 Appendix F: JIDA Standard

21.1 Calling Convention

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jumptec Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

- AH=EAh
- AL=function number
- DX=4648h (security word)
- CL=board number (starting with 1)

The interrupt returns a CL≠0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

21.2 Obtaining JIDA Information

To obtain information about boards that follow the JIDA standard:

- Call Get BIOS ID with CL=1.
  The name of the first device installed will be returned.
  If you see the result Board exists (CL=0), increment CL, and call Get BIOS ID again.
- Repeat until you see Board not present (CL≠0).
  You now know the names of all boards within your system that follows the JIDA standard.
- You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

Note: *Association between board and board number may change because of configuration changes. Do not rely on associations between board and board number. Use the above procedure to determine the association between board and board number.*

Refer to the JIDA manual in the jidai110.zip folder, which is available from the Kontron Web site, for further information on implementing and using JIDA calls with C sample code.

22 Appendix G: JUMPTEC Remote Control

The JUMPtec Remote Control (JRC), an extension of the PC BIOS, provides a way to intercept and reroute BIOS functionality over a serial port at an early stage during booting.

There are two software components involved:

- The BIOS extension. The PC that contains this component is referred to as a client. This component is part of the JUMPtec (Kontron) Extension BIOS.
- Application. The second component runs on a different machine, referred to as host, and is connected with a serial cable to a client. The second component is an application that can run at the command prompt or from batch files. The component is available as a 32-bit Windows console for Windows 9x or NT and as an MS-DOS application.

You can configure the interception in one of two ways:

- Server Mode provides a way of intercepting screen output from and keyboard input to the client on the host machine. In Server Mode, you can map the host's floppy drive to the client's drive-specifier A:. The host also can emulate a single disk drive as a file on the host machine's hard disk. Create this file using the command IMGCREATE. The file is accessible from the client machine as Drive A:.
- Image Mode allows you to halt the boot process of the client. This allows the host machine to read or write the contents of the CMOS RAM, EEPROM CMOS mirror, and NVRAMs of other Kontron boards as well as the contents of flash, hard, or floppy disks of the client.

For further information, see Application Note JRCUsage_E113.pdf, which is available from the Kontron Web site under Tech Support.

23 Appendix H: PC Architecture Information

The following sources of information can help you better understand PC architecture.

23.1 Buses

23.1.1 ISA, Standard PS/2 - Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

23.1.2 PCI/104

- Embedded PC 104 Consortium
  The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
  The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- *PCI System Architecture,* Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

23.2 General PC Architecture

- *Embedded PCs*, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- *Hardware Bible*, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- *Interfacing to the IBM Personal Computer*, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9

- *The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition*, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

23.3 Ports

23.3.1 RS-232 Serial

- EIA-232-E standard
  The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- *RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems*, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor
  The Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

23.3.2 Serial ATA

- Serial AT Attachment (ATA) Working Group
  This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.
  We recommend you also search the Web for information on *4.2 I/O cable*, if you use hard disks in a DMA3 or PIO4 mode.

23.3.3 USB

- USB Specification
  USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

23.4 Programming

- *C Programmer’s Guide to Serial Communications*, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- *Programmer's Guide to the EGA, VGA, and Super VGA Cards*, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4

- *The Programmer's PC Sourcebook,* Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- *Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas*, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

24 Appendix I: Document Revision History

Version	Date	Edited by	Changes
1.0	24.08.98	MH	Manual created.
2.0	21.07.00	BJ	Updated to HW rev. 2.0.
2.1	13.11.00	BJ	Added IRQ10 for onboard Ethernet, and information on D201LCD cmd-line parameters.
2.2	29.11.00	BJ	Added parts list for Ethernet cable.
2.3	04.06.01	CC	Updated with new template and format. Reorganized and updated all sections.
2.4	10.07.01	CH	Changed environmental specification, minor changes.
2.5	23.11.01	JL	Formatting and editing updates throughout.
2.6	21.01.02	UMA	Update information on DMA channels.
2.7	11.08.03	GDA and JL	Technical updates, formatting and editing updates throughout.
2.8	26.04.06 27.04.06	GUL GUL	Updated contact addresses Changed to new Kontron style Released for Web
2.9	23.04.07	GUL	Updated to new Kontron style